CLAIMS

What is claimed is:

1. A method of synchronizing a local timing signal with a clock signal, the method comprising:

delaying a clock signal in response to at least a first control signal to generate a first delayed clock signal;

delaying the first delayed clock signal in response to at least a second control signal to generate a second delayed clock signal; and

generating a timing signal synchronized to the clock signal in response to the first and second delayed clock signals.

2. The method of claim 1, wherein generating a timing signal synchronized to the ~~timing~~ clock signal comprises:

generating a rising edge of the timing signal in response to the first delayed clock signal; and

generating a falling edge of the timing signal in response to the second delayed clock signal.

3. The method of claim 2, wherein the rising edge of the timing signal is generated in response to a rising edge of the first delayed clock signal.

4. The method of claim 2, wherein the falling edge of the timing signal is generated in response to a rising edge of the second delayed clock signal.

5. The method of claim 1, further comprising:

comparing a signal representative of the timing signal with the clock signal; and

generating the at least a first control signal in response to a phase difference between the clock signal and the signal representative of the timing signal.

6. The method of claim 5, wherein generating the synchronized timing signal further comprises phase-locking a rising edge of the clock signal with a rising edge of the timing signal when the phase difference is substantially zero.

7. The method of claim 6, further comprising generating a phase-lock signal in response to phase-locking the rising edges of the clock signal and the timing signal.

8. The method of claim 7, further comprising:

comparing a signal representative of an inverse of the timing signal with an inverse of the clock signal; and

generating the at least a second control signal in response to a phase difference between the signal representative of the inverse of the timing signal and the inverse of the clock signal.

9. The method of claim 8, further comprising phase-locking a falling edge of the clock signal with a falling edge of the ~~local~~ timing signal when the phase difference is substantially zero.

10. The method of claim 8, wherein comparing the signal representative of an inverse of the timing signal with an inverse of the clock signal is initiated in response to a rising edge of the clock signal being phase-locked with a rising edge of the timing signal.

11. The method of claim 1, further comprising:

generating an inverse clock signal; and

generating a timing signal synchronized to the inverse clock signal in response to the first and second delayed clock signals.

12. A method of generating a timing signal, the method comprising:

delaying a clock signal in response to at least a first control signal;

delaying the delayed clock signal in response to at least a second control signal to establish at least one twice delayed clock signal; and

generating a timing signal in response to the at least one twice delayed clock signal.

13. The method of claim 12, wherein delaying the delayed clock signal comprises:

generating an inverse of the delayed clock signal;

delaying the delayed clock signal by a fixed number of delays; and

delaying the inverse of the delayed clock signal by a variable number of delays.

14. The method of claim 13, wherein generating a timing signal in response to the twice delayed clock signal comprises:

generating a rising edge of the timing signal in response to the delayed clock signal delayed by a fixed number of delays; and

generating a falling edge of the timing signal in response to the inverse of the delayed clock signal delayed by a variable number of delays.

15. The method of claim 13, further comprising varying the variable number of delays in response to the at least a second control signal.

16. The method of claim 12, further comprising generating the at least a second control signal in response to a phase difference between an inverse of the clock signal and an inverse of a signal representative of the timing signal.

17. A data synchronizing circuit comprising:

at least two operably coupled phase detectors, each phase detector configured to generate at least one control signal in response to at least one signal representative of a system clock signal, at least one signal representative of a local timing signal and at least one initialization signal; and

circuitry coupled to the at least two phase detectors and configured to generate a timing signal synchronized with the system clock signal.

18. The data synchronizing circuit of claim 17, wherein a first of the at least two phase detectors is coupled to a first delay circuit, the first delay circuit being coupled to a signal line configured to receive a signal representative of the system clock signal, and wherein a second of the at least two phase detectors is coupled to a second delay circuit, the second delay circuit being coupled to the first delay circuit and to the circuitry configured to generate the timing signal.

19. The data synchronizing circuit of claim 17, further comprising circuitry coupled to the first and second delay circuits, ~~the circuitry~~ configured to create at least one signal in response to at least one of a rise and a fall in at least one signal generated by at least one of the first and second delay circuits.

20. The data synchronizing circuit of claim 19, wherein the circuitry coupled to the first delay circuit is coupled through a third delay circuit.

21. The data synchronizing circuit of claim 20, wherein the third delay circuit is configured to delay a signal a fixed number of delays.

22. The data synchronizing circuit of claim 18, wherein the second delay circuit is coupled to the first delay circuit through a signal inverter.

23. An electronic system comprising:

a processor;

a memory device associated with the processor; and

at least one of an input device, an output device and a data storage device associated with the processor;

wherein at least one component of the electronic system comprises a data synchronizing circuit comprising:

at least two operably coupled phase detectors, each phase detector configured to generate at least one control signal in response to at least one signal representative of a system clock signal, ~~the~~ at least one signal representative of a local timing signal and at least one initialization signal; and

circuitry coupled to the at least two phase detectors and configured to generate a data timing signal synchronized to the system clock signal in response to outputs from each of the at least two phase detectors.

24. A semiconductor substrate comprising structures configured to synchronize data to a system clock signal, the structures comprising:

at least two operably coupled phase detectors, each phase detector configured to generate at least one control signal in response to at least one signal representative of a system clock signal, ~~the~~ at least one signal representative of a local timing signal and at least one initialization signal; and

circuitry coupled to the at least two phase detectors and configured to generate a data timing signal synchronized to the system clock signal in response to outputs from each of the at least two phase detectors.